METHOD AND LATCH CIRCUIT FOR IMPLEMENTING ENHANCED PERFORMANCE WITH REDUCED QUIESCENT POWER DISSIPATION USING MIXED THRESHOLD CMOS DEVICES

Abstract of the Disclosure

A method and latch circuit are provided for implementing enhanced performance with reduced quiescent power dissipation using mixed threshold CMOS devices. A latch circuit includes critical data and clock paths and non-critical sections. A low voltage threshold (LVT) transistor is used only in the critical data and clock paths. The non-critical sections are implemented with regular VT, (RVT), or low leakage (LLD) transistors. The latch circuit advantageously is implemented using LVT devices in the internal critical paths of the latch and RVT output buffer transistors.